

Integrated Power Passives for Lightweight Low-Power Space Applications

Grant Category: Space-Based Research and Payload Development

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1. Objective: The goal of this research project is to leverage IC fabrication and MEMS technology to develop high-energy-density integrated passives (i.e., inductors and capacitors) to achieve systems-on-a-chip (SoCs) with small form factor, low power consumption, better thermal handling, and improved reliability. Thus the payload in space vehicles can be significantly increased without increasing the cost. Specifically, the effort will be focused on developing an integratable ultra-high-density (UHD) metal-insulator-metal (MIM) capacitor. The objective is to improve the capacitance density by a factor of at least 20, and thus reduce the footprint of capacitors by the same amount.

2. Problems of existing solutions: Ferroelectric materials with high dielectric constants have been explored to make high-density capacitors, but their dielectric constants vary with temperature and frequency. They also require high-temperature treatment which makes them incompatible with CMOS processes. Stacking multiple capacitor layers seems to be an obvious alternative way to increase capacitance density. However, adding one layer requires adding one photomask for interconnection. Two to three layers have been demonstrated, but it is getting too expensive and eventually becomes impractical when the number of capacitor layers exceeds 10. Therefore, the big challenge is how to interconnect 10's or even 100's of capacitor layers with a small number of photomasks (<5).

3 Proposed solution: In this project, a novel fabrication process is proposed, in which only three photomasks are needed to interconnect a large number (e.g., 50) of layers and the fabrication process is CMOS compatible. This process is enabled by three key innovative techniques:

- (1) Fabrication of coplanar multiple layers. This novel approach utilizes the fact that multiple thin-film layers consecutively deposited pile side by side at vertical sidewalls. Then all the layers are exposed in a single horizontal plane after the top of the sidewalls is polished. At this point, regular photolithography can apply if the layer thicknesses are greater than the photolithographic limit.
- (2) Nano-scale fabrication. For ultra-high-density (UHD) capacitance, the thicknesses of the thin-film layers may be just in order of 10 nm or less. No standard photolithographic techniques yet can achieve such small feature sizes. The proposed nanofabrication technique uses selective etching to connect the electrodes of capacitors.
- (3) High-k dielectric material deposition. A unique ultraviolet-enhanced pulsed laser deposition (UV-PLD) system will be used.

Therefore, multiple capacitor layers are connected with merely three masks. The process is CMOS-compatible. One of the most intriguing advantages of this proposed method is that it simply provides kind of a capacitance multiplier. Other capacitance density enhancement approaches such as V-grooves, high-k dielectrics and high-k ceramics all can be directly combined with this new technology to boost the capacitance density by orders of magnitude. Moreover, any material performance improvement or new material discoveries can be immediately adopted in this technology.

4. Potential applications of the proposed technology:

Attributed to the high-capacitance density and CMOS compatibility, the proposed UHD capacitors can be integrated or discrete components that can have significant impacts in the following applications:

- Power system-on-a-chip (SoC) and power management. For example, truly monolithic power converters with all passives integrated, as illustrated in Fig. 1, can be realized with a small footprint. The integrated UHD capacitors will not only reduce the form factor of the capacitors themselves, but also will significantly decrease the printed-circuit-board (PCB) area or eventually completely eliminate the PCB.
- Integrated UHD capacitors for decoupling and sampling in wireless applications.
- Discrete UHD capacitors for system-in-package (SIP) and PCB applications.
- High-voltage, high-energy-density power storage devices.
- Nano air vehicles (NAV). High density integration is the key.
- All above devices can be applied to space applications for lightweight, low power, and low cost.
- Nanoscale fabrication. Nanowires or structures with nanometers can be made without using expensive or time-consuming nanofabrication equipment.

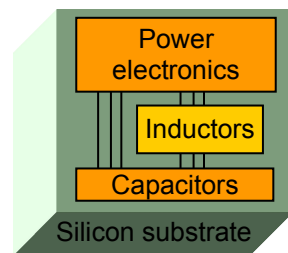


Figure 1. Conceptual illustration of a monolithic power converter.